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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,936	10/22/2003	Takashi Ohsumi	IIZ.003D2C	4027
7590 12/23/2004 VOLENTINE FRANCOS, P.L.L.C. SUITE 150 12200 SUNRISE VALLEY DRIVE RESTON, VA 20191			EXAMINER TOLEDO, FERNANDO L	
			ART UNIT 2823	PAPER NUMBER

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/689,936

Applicant(s)

OHSUMI, TAKASHI

Examiner

Fernando L. Toledo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 22 October 2003.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 22-30 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 22-30 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 22 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☒ Certified copies of the priority documents have been received in Application No. 08/959,667.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 10/22/03 & 4/02/04.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date: \_\_\_\_\_  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Information Disclosure Statement*

1. The information disclosure statements (IDS) submitted on 22 October 2003 and 2 April 2004 have been considered by the Examiner.

### *Double Patenting*

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefore ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

3. Claims 24 and 29 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1 and 3 of prior U.S. Patent No. 6,713,319. This is a double patenting rejection.

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 22, 23, 25, 27 and 28 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 – 3 of U.S. Patent No. 6,713,319. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 22 and 27 of the present invention are generic with respect to the patented claims 1 and 3 of the US Patent No. 6,713,319. A species claim anticipates a generic claim; therefore, the patented claim anticipates the examined claim. See MPEP 806.04 (i).

*Claim Rejections - 35 USC § 103*

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 22, 23, 25 – 27 and 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Frye (U. S. Patent 5,534,465) in view of Yamada et al. (U. S. Patent 5,864,178).

In re claim 22, Frye in the U. S. Patent 5,534,465; figures 1 – 5 and related text, discloses fabricating a semiconductor substrate 20 having a first surface in which a semiconductor integrated circuit is formed (Figure 4); the semiconductor substrate including a conductive layer 36 formed on the first surface thereof which is connected to the semiconductor integrated circuit and including a base member 35 of insulating material arranged between the first surface and the conductive layer; the base member including a first surface facing the first surface of the semiconductor substrate and a second surface opposite the first surface of the base member

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(Figure 4); the conductive layer having an extended portion extending on the surface of the base member (Figure 4); providing a connection substrate 40 on which the semiconductor substrate is to be mounted; placing the semiconductor substrate so that the first surface of the semiconductor substrate faces the connection substrate (Figure 4); connecting the extended portion of the conductive layer to the connection substrate (Figure 4).

Frye does not show supplying a seal member in a space between the semiconductor substrate and the connection substrate.

Yamada, in the U. S. Patent 5,864,178; figures 1 – 79 and related text, discloses supplying a seal member in a space between the semiconductor substrate and the connection substrate to reduce the shear strain  $\gamma_{\max}$  to be generated at the bump electrode (Column 1, Lines 36 – 67 and Column 2, Lines 1 – 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supply a seal member in a space between the semiconductor substrate and the connection substrate, in the invention of Frye, since, as taught by Yamada, it reduces the shear strain  $\gamma_{\max}$  to be generated at the bump electrode.

8. In re claim 23, Frye discloses wherein the first surface of the semiconductor substrate is placed to face the connection substrate using a face down technique (Figure 4).

9. In re claim 25, Frye discloses wherein the conductive layer and the base member constitute an electrode (Figure 4).

10. In re claim 26, Yamada teaches wherein the seal member has a first surface, and has a second surface opposite the first surface of the seal member, the first surface of the seal member being provided on the first surface of the semiconductor substrate, and the second surface of the

seal member being provided as coplanar with an upper surface of the extended portion of the conductive layer (Column 21, Lines 46 – 62 and Figure 11).

11. In re claim 27, Frye discloses fabricating a semiconductor substrate 20 having a first surface in which a semiconductor integrated circuit is formed (Figure 4); the semiconductor substrate including a conductive layer 36 formed on the first surface thereof which is connected to the semiconductor integrated circuit and including a base member 35 of insulating material arranged between the first surface and the conductive layer; the base member including a first surface facing the first surface of the semiconductor substrate and a second surface opposite the first surface of the base member (Figure 4); the conductive layer having an extended portion extending on the surface of the base member (Figure 4); providing a connection substrate 40 on which the semiconductor substrate is to be mounted; placing the semiconductor substrate so that the first surface of the semiconductor substrate faces the connection substrate (Figure 4); connecting the extended portion of the conductive layer to the connection substrate (Figure 4).

Frye does not show supplying a seal member in a space between the semiconductor substrate and the connection substrate.

Yamada, discloses supplying a seal member in a space between the semiconductor substrate and the connection substrate to reduce the shear strain  $\gamma_{\max}$  to be generated at the bump electrode (Column 1, Lines 36 – 67 and Column 2, Lines 1 – 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supply a seal member in a space between the semiconductor substrate and the connection substrate, in the invention of Frye, since, as taught by Yamada, it reduces the shear strain  $\gamma_{\max}$  to be generated at the bump electrode.

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12. In re claim 30, Yamada teaches wherein the seal member has a first surface, and has a second surface opposite the first surface of the seal member, the first surface of the seal member being provided on the first surface of the semiconductor substrate, and the second surface of the seal member being provided as coplanar with an upper surface of the extended portion of the conductive layer (Column 21, Lines 46 – 62 and Figure 11).

### ***Claim Objections***

13. Claim 29 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 29 is dependent on claim 28. Claim 28 states the following limitation “wherein the base member and the sealing member are a same material.” Therefore, if both members are made of the same material they will have the same thermal expansion coefficient, since the thermal expansion coefficient is an inherent property of the material regardless of what it is used for.

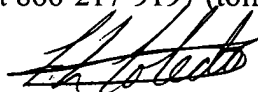
### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando L. Toledo whose telephone number is 571-272-1867. The examiner can normally be reached on Mon-Thu 7am to 5:30pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Fernando L. Toledo  
Examiner  
Art Unit 2823

FLT  
16 December 2004